# RESISTANCE AND CAPACITANCE ESTIMATION

## ABSTRACT OF THE DISCLOSURE

A method of designing a VLSI chip and a chip designed according to the method are described. The method includes the steps of early consideration of resistive and capacitive values during a VLSI chip design process. The method provides for estimation of signal routes between nodes of functional blocks to be incorporated in the chips. The estimation may be based on a floor plan describing the positioning of the functional blocks, a connectivity description identifying connections between ports of the blocks and physical and mechanical configuration parameters. The functional blocks and design of the layout may be hierarchical in nature. The signal route estimation may be based on control factors such as the specification of signal route establishment algorithms. The next step is to foliate the nodes followed by determining resistance and capacitance values corresponding to all or parts of the estimated signal routes. The resistive and capacitive values may be incorporated into a model and a connectivity net list may be generated.